1. A method to generate an optimum phase shifted sampling clock for sampling a synchronized video signal A(t) having a synchronization signal SYNC pulse, said method comprising:

generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse wherein said sampling clock period comprises said SYNC pulse period divided by M;

counting the number of sampling clock cycles N from said trailing edge of said SYNC pulse until said A(t) value at said first edge of said sampling clock exceeds a minimum value;

thereafter phase shifting said sampling clock and said SYNC pulse forward until said A(t) value at said first edge of said sampling clock first exceeds a minimum value on clock cycle N-1 to thereby establish a worst case phase shift of said sampling clock; and

thereafter sampling said A(t) at an offset from said worst case phase shift to thereby generate an optimum phase shifted sampling clock.

2. The method according to Claim 1 further comprising

canceling signal jitter in said SYNC pulse prior to said step of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse.

3. The method according to Claim 1 wherein said step of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse comprises a phase lock loop.

4. The method according to Claim 1 wherein said step of phase shifting said sampling clock and said SYNC pulse comprises discrete units of time.

5. The method according to Claim 1 wherein said SYNC pulse comprises a horizontal synchronization pulse and M comprises a number of pixels on each horizontal line of a digital display.

6. The method according to Claim 1 wherein said offset comprises 1/2 of said sampling clock period.

7. The method according to Claim 1 wherein said offset comprises 3/4 of said sampling clock period.

8. The method according to Claim 1 wherein said synchronized video signal A(t) comprises a VGA format video signal.

9. The method according to Claim 1 wherein said first edge of said sampling clock comprises a rising edge.

10. A method to generate an optimum phase shifted sampling clock for sampling a synchronized video signal A(t) having a synchronization signal SYNC pulse, said method comprising:

generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse wherein said sampling clock period comprises said SYNC pulse period divided by M;

counting the number of sampling clock cycles N from said trailing edge of said SYNC pulse until said A(t) value at said first edge of said sampling clock exceeds a minimum value;

thereafter phase shifting said sampling clock and said SYNC pulse forward until said A(t) value at said first edge of said sampling clock first exceeds a minimum value on clock cycle N-1 to thereby establish a worst case phase shift of said sampling clock; and

thereafter sampling said A(t) at an offset from said worst case phase shift to thereby generate an optimum phase shifted sampling clock wherein said offset comprises a fraction of said sampling clock period.

11. The method according to Claim 10 further comprising canceling signal jitter in said SYNC pulse prior to said step of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse.

12.The method according to Claim 10 wherein said step of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse comprises a phase lock loop.

13.The method according to Claim 10 wherein said step of phase shifting said sampling clock and said SYNC pulse comprises discrete units of time.

14.The method according to Claim 10 wherein said SYNC pulse comprises a horizontal synchronization pulse and M comprises a number of pixels on each horizontal line of a digital display.

15.The method according to Claim 10 wherein said synchronized video signal A(t) comprises a VGA format video signal.

16.The method according to Claim 10 wherein said first edge of said sampling clock comprises a rising edge.

17.An optimized phase shifted sampling clock circuit for sampling a synchronized video signal A(t) having a synchronization signal SYNC pulse, said circuit comprising:

a means of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse wherein said sampling clock period comprises said SYNC pulse period divided by M;

a means of counting the number of sampling clock cycles N from said trailing edge of said SYNC pulse until said A(t) value at said first edge of said sampling clock exceeds a minimum value;

a means of phase shifting said sampling clock and said SYNC pulse forward until said A(t) value at said first edge of said sampling clock first exceeds a minimum value on clock cycle N-1 to thereby establish a worst case phase shift of said sampling clock; and

a means of sampling said A(t) at an offset from said worst case phase shift to thereby generate an optimum phase shifted sampling clock.

18. The circuit according to Claim 17 further comprising a means of canceling signal jitter in said SYNC pulse.

19. The circuit according to Claim 17 wherein said means of generating a sampling clock having a first edge aligned with a trailing edge of said SYNC pulse comprises a phase lock loop.

20. The circuit according to Claim 17 wherein said means of phase shifting said sampling clock and said SYNC pulse comprises discrete units of time.

21. The circuit according to Claim 17 wherein said SYNC pulse comprises a horizontal synchronization pulse and M comprises a number of pixels on each horizontal line of a digital display.

22. The circuit according to Claim 17 wherein said offset comprises 1/2 of said sampling clock period.

23.The circuit according to Claim 17 wherein said offset comprises 3/4 of said sampling clock period.

24. The circuit according to Claim 17 wherein said offset comprises a fraction of said sampling period wherein said fraction can be any value between about 0 and 1.

25. The circuit according to Claim 17 wherein said synchronized video signal A(t) comprises a VGA format video signal.

26. The circuit according to Claim 17 wherein said first edge of said sampling clock comprises a rising edge.